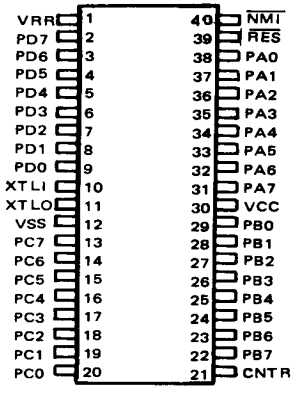
6500/1 and 6500/1E
SINGLE-CHIP MICROCOMPUTER

- **6502 CPU**
  - 8-bit parallel processing
  - Software upward / downward compatibility
  - 13 addressing modes
  - Decimal or binary arithmetic
  - True indexing capability
  - Memory addressable I/O
  - Pipeline architecture
- **2048 x 8 mask-programmable ROM**
- **64 x 8 static RAM**
- **Power down mode**
- **32 bidirectional TTL compatible I/O lines (1 positive and 1 negative edge sensitive)**
- **1 bidirectional TTL compatible counter I/O line**
- **16-bit programmable counter / latch**
  - Interval timer
  - Pulse generator
  - Event counter
  - Pulse width measurement
- **Five interrupts: 4 external and 1 counter overflow**
- **4 MHz max crystal or external clock frequency**
- **1 or 2 MHz internal clock**
- **70% of instructions have execution times less than 2 μs at 2 MHz**
- **NMOS silicon gate, depletion load technology**
- **Single +5V power supply**
- **Emulator device available (NCR 6500/1E)**

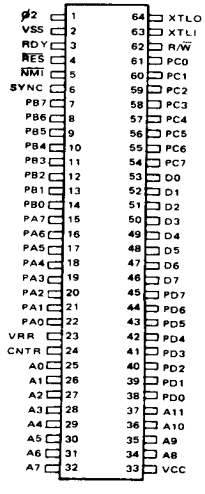
The NCR 6500/1 is a complete, high-performance 8-bit microcomputer on a single chip. It is software compatible with all members of the 6502 and 6500 families. The NCR 6500/1 consists of a 6502 CPU, an internal clock oscillator, 2048 bytes of ROM, 64 bytes of RAM and versatile interface circuitry. The interface circuitry includes a 16-bit programmable counter / latch, 32 bidirectional I/O lines (including 2 edge-sensitive lines), 5 interrupts and 1 counter I/O line.

To aid in designing NCR 6500/1 microcomputer systems, NCR offers a ROM-less PROM-compatible emulator device, the NCR 6500/1E. The architecture of the emulator device is the same as that of the NCR 6500/1, except that the NCR 6500/1E provides 24 additional signals to route the address bus (12 lines), the data bus (8 lines), and control signals (4 lines) off the chip for connection to memory.

PIN CONFIGURATION

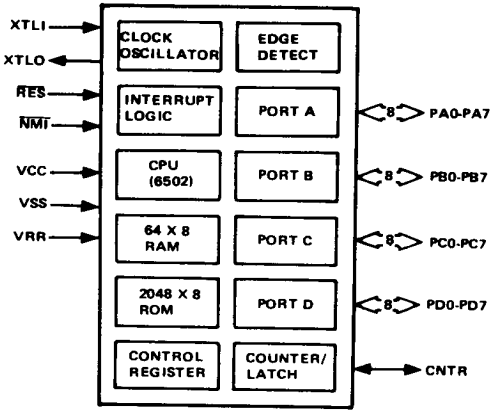


NCR6500/1



NCR6500/1E

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin Name	Pin Number	Description
VCC	30	Main power supply + 5V
VRR	1	Separate power pin for RAM. In the event that VCC power is lost, this power retains RAM data.
VSS	12	Signal ground
XTLI	10	Crystal, clock or RC network input for internal clock oscillator.
XTLO	11	Crystal or RC network ouput from internal clock oscillator.
$\overline{RES}$	39	The Reset input is used to initialize the NCR6500/1. This signal must not transition from low to high for at least eight cycles after VCC reaches operating range and the internal oscillator has stabilized.
$\overline{NMI}$	40	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated within the CPU.
PA0-PA7 PB0-PB7 PC0-PC7 PD0-PD7	38-31 29-22 20-13 9-2	Four 8-bit ports used for either input/output. Each line consists of an active transistor to VSS and a passive pull-up to + 5V. The two lower bits of the PA port(PA0 and PA1) also serve as edge detect inputs with maskable interrupts.
CNTR	21	This line is used as a Counter input/output line. CNTR is an input in the Event Counter and Pulse Width Measurement modes and is an output in the Interval Timer and Pulse Generator modes.

NOTE: All NCR 6500/1 interface signals are provided in the NCR 6500/1E. While the interface electrical characteristics are identical, the NCR 6500/1E pin assignments are different from the NCR 6500/1 in order to accomodate the 64-pin emulator package.

ADDITIONAL NCR 6500/1E PIN DESCRIPTIONS

Pin Name	Pin Number	Description
RDY	3	Ready. The Ready input delays execution of any cycle during which the RDY line is low. This allows the user to halt or single step the CPU on any cycle except a write cycle. A negative transition to the low state during the $\phi 2$ clock low pulse will halt the CPU with the address lines containing the current address being fetched. If RDY is low during a write cycle, it is ignored until the following read operation. This condition will remain through a subsequent $\phi 2$ clock pulse in which the RDY line is low.
SYNC	6	Sync. The Sync signal is provided to identify those cycles in which the CPU is performing an OP CODE fetch. SYNC goes high during $\phi 2$ clock-low pulse during an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the $\phi 2$ clock low pulse in which SYNC went high, the CPU will halt in its current state and will remain in that state until the RDY line goes high. Using this technique, the SYNC signal can be used to control RDY to cause single instruction execution.
$\phi 2$	1	Phase 2 ($\phi 2$) clock pulse. Data transfer can take place only during $\phi 2$ clock pulse.
A0-A11	25-32 34-37	Address Bus Lines. The address bus buffers on the NCR6500/1E are push/pull type drivers capable of driving at least 130 pf and one standard TTL load. The address bus always contains known data. The addressing technique involves putting an address on the address bus which is known to be either in program sequence, on the same page in program memory, or at a known point in memory. The I/O addresses are also placed on these lines.
D0-D7	53-46	Data Bus Lines. All transfers of instructions and data between the CPU and external memory take place on the data bus lines. The buffers driving the data bus lines have full three-state capability. Each data bus pin is connected to an input and an output buffer, with the output buffer remaining in the floating condition.
R/W	62	Read/Write. The Read/Write output controls the direction of data transfer between the NCR6500/1E Emulator CPU and external memory. This line is high when reading data from memory and low when writing data to memory.

DEVICE OPERATION

CENTRAL PROCESSING UNIT (CPU)

The CPU in the NCR 6500/1 and NCR 6500/1E is a standard 6500 configuration with the standard 6500 instructions. All instructions are executed in 2 to 7 clock cycles. The automatic increment/decrement feature of the stack pointer facilitates rapid and flexible subroutine execution and interrupt servicing, including context switching. Two 8-bit index registers permit pre- and post-indexing of indirect addresses. (For details on the CPU operation, see NCR 6500/1 and NCR 6500/1E Data Sheet, Publication Number MC—700).

READ ONLY MEMORY (ROM)

The ROM for the NCR 6500/1 consists of 2048 by 8 bits of mask-programmable memory with an address space from 800 to FFF. The NCR 6500/1E has no ROM.

RANDOM ACCESS MEMORY (RAM)

The RAM for the NCR 6500/1 and NCR 6500/1E consists of 64 by 8 bits of read/write memory. In order to take advantage of efficient zero page addressing capabilities, the RAM is assigned addresses 0 to 03F. A standby power pin, VRR allows RAM memory to be maintained at less than 10% of the operating power in the event that VCC power is lost.

CLOCK OSCILLATOR

The clock oscillator provides the basic timing signals used by the CPU. The reference frequency is provided by an external source, and can be from a crystal, clock or RC network input. The RC network mode is a mask option. (The external frequency reference of the NCR 6500/1E may be a crystal or a clock; the RC option is not available on this emulator device.) The external frequency can vary from 200 KHz to 4 MHz. The internal Phase 2 ($\phi 2$) frequency is one-half the external reference frequency. A 4.7K ohm resistor will provide nominal 2 MHz oscillation and 1 MHz internal operation in the RC mask option ± 35%).

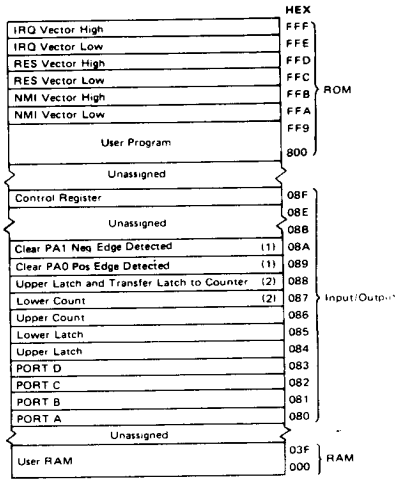
BIDIRECTIONAL I/O PORTS

The NCR 6500/1 and NCR 6500/1E provide four 8-bit I/O ports (PA, PB, PC, and PD). Associated with the I/O ports are four 8-bit registers located on page zero. (See System Memory Maps for specific addresses.) Each I/O line is individually selectable as an input or an output.

COUNTER / LATCH

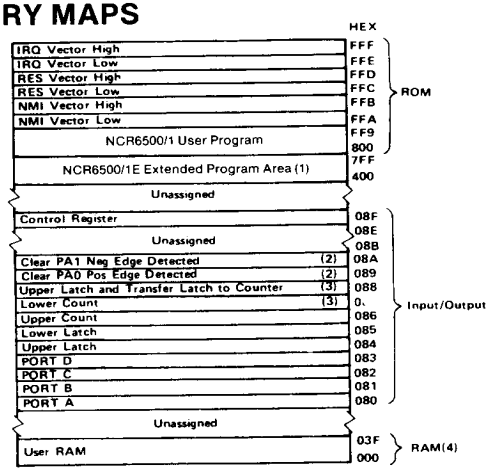
The Counter / Latch consists of a 16-bit decrementing counter and a 16-bit latch. The counter and the latch are each comprised of two 8-bit registers. The counter operates in any of four modes: Interval Timer, Pulse Generator, Event Counter, or Pulse Width Measurement.

DETAILED MEMORY MAPS



Notes:
(1) I/O command only; i.e., no stored data.
(2) Clears Counter Overflow – Bit 7 in Control Register

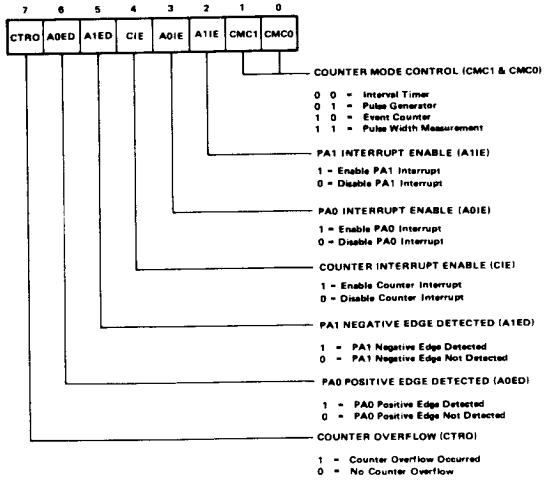
NCR 6500/1



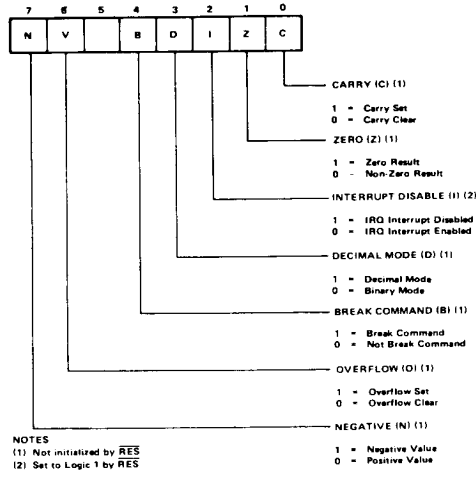
NOTES
(1) Additional 1024 bytes are decoded for external memory addressing by the NCR6500/1E Emulator Device. This area can be used during debug, but cannot be used in a masked ROM NCR6500/1.
(2) I/O command only; i.e., no stored data.
(3) Clears Counter Overflow - Bit 7 in Control Register.
(4) CAUTION: The NCR6500/1E allows RAM mapping into o40-07F, 100-13F, 140-17F, 200-23F, 240-27F, 300-33F, and 340-37F; as well as 000-03F. The production NCR6500/1, however allows RAM mapping only at 000-03F.

NCR 6500/1E

KEY REGISTER SUMMARY



Control Register



NOTES
(1) Not initialized by $\overline{RES}$
(2) Set to Logic 1 by $\overline{RES}$

Processor Status Register

ELECTRICAL SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{in}	−0.3 to +7.0	Vdc
Operating Temperature Range	T_A		°C
Commercial		0 to +70	
Industrial		−40 to +85	
Storage Temperature Range	T_{stg}	−55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

D.C. CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Dissipation (Outputs High)	P_D				mW
0°C to +70°C (NCR 6500/1)		—	500	—	
−40°C to +85°C (NCR 6500/1)		—	550	—	
0°C to +70°C (NCR 6500/1E)		—	750	1200	
RAM Standby Voltage (Retention Mode)	V_{RR}	3.5	—	V_{CC}	Vdc
RAM Standby Current (Retention Mode)	I_{RR}				mAdc
0°C to +70°C		—	10	—	
−40°C to +85°C		—	12	—	
Input High Voltage (PA, PB, PC, CNTR, $\overline{RES}$, $\overline{NMI}$)	V_{IH}	+2.0	—	V_{CC}	Vdc
Input Low Voltage (PA, PB, PC, CNTR, $\overline{RES}$, $\overline{NMI}$)	V_{IL}	−0.3	—	+0.8	Vdc
Input Leakage Current	I_{IN}				μAdc
V_{in} = 0 to 5.0 Vdc $\overline{RES}$, $\overline{NMI}$				±10	
Input High Voltage (XTLI)	V_{IHXT}	+4.0	—	V_{CC}	Vdc
Input Low Voltage (XTLI)	V_{ILXT}	−0.3	—	+0.8	Vdc
Input Low Current	I_{IL}				
(V_{IL} = 0.4 Vdc)		—	−1.0	−1.6	mAdc
Output High Voltage	V_{OH}				
(V_{CC} = min, I_{Load} = −100 uAdc)		−2.4	—	—	Vdc
Output High Voltage	V_{CMOS}	V_{CC}−30%	—	—	Vdc
(V_{CC} = min)					
Output Low Voltage	V_{OL}				
(V_{CC} = min, I_{Load} = 1.6 mAdc)		—	—	+0.4	Vdc
Output High Current (Sourcing)	I_{OH}				
(V_{OH} = 2.4 Vdc)		−100		—	μAdc
Output Low Current (Sinking)	I_{OL}				
(V_{OL} = 0.4 Vdc)		1.6	—	—	mAdc
Input Capacitance	C_{in}				pF
(V_{in} -0, T_A = 25°C, f = 1.0 MHz)					
PA, PB, PC, PD CNTR		—	—	10	
XTLI, XTLO		—	—	50	
Output Capacitance	C_{out}				
(V_{in} -0, T_A = 25°C, f = 1.0 MHz)		—	—	10	pF
I/O Port Pull-up Resistance (Optional)	R_L	3.0	6.0	11.5	KΩ
PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7, CNTR					

NOTE: Negative sign indicates outward current flow, positive indicates inward flow. Unless otherwise indicated, characteristic refers to PA, PB, PC, PD and CNTR signals.

A.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V)

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
XTLI Input Clock Cycle Time	T_{cyc}	0.500	5.0	0.250	5.0	μ sec
Internal Write to Peripheral Data Valid (TTL)	T_{PDW}	1.0		0.5		μ sec
Internal Write to Peripheral Data Valid (CMOS)	T_{CMOS}	2.0		1.0		μ sec
Peripheral Data Setup Time	T_{PDSU}	400		200		nsec
Count and Edge Detect Pulse Width	T_{PW}	1.0		0.5		μ sec

NCR 6500/1E ELECTRICAL SPECIFICATIONS

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Threshold Voltage D0-D7, RDY,	V_{IHT}	V_{SS} + 2.4	–	–	Vdc
Input Low Threshold Voltage D0-D7, RDY,	V_{ILT}	–	–	V_{SS} + 0.8	Vdc
Three-State (Off State) Input Current (V = 0.4 to 2.4V, V_{CC} = 5.25V) D0-D7	I_{TSI}		–	10	µA
Output High Voltage (I_{LOAD} = 100µ Adc, V_{CC} = 4.75V) D0-D7, SYNC, A0-A11, R/$\overline{W}$, ϕ2	V_{OH}	V_{SS} + 2.4	–	–	Vdc
Output Low Voltage (I_{LOAD} = 1.6 mAdc, V_{CC} = 4.75V) D0-D7, SYNC, A0-A11, R/$\overline{W}$, ϕ2	V_{OL}		–	V_{SS} + 0.6	Vdc
Capacitance (V_{in} = 0, T_A = 25°C, f = 1 MHz) RDY D0-D7 A0-A11, R/$\overline{W}$, SYNC ϕ2	C C_{in} C_{out} $C_{\phi 2}$	– –	– – – 50	10 15 12 80	pF

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